THE SMART BACKPLANE – LOWERING THE COST OF SPACECRAFT AVIONICS BY IMPROVING THE RADIATION TOLERANCE OF COTS ELECTRONIC SYSTEMS

Daniel Gleeson, MSc.
Curtiss-Wright, dgleeson@curtisswright.com

Milos Melicher, MSc.
Curtiss-Wright, mmelicher@curtisswright.com

ABSTRACT

The lowering of the cost of access to space while maintaining mission assurance is something everyone is interested in from system integrators to funding agencies and spacecraft operators. Engineers at Curtiss-Wright have developed an innovative approach to lowering the costs of achieving space mission objectives by developing in-situ radiation induced latch-up protection of existing non-space COTS electronics boards for spacecraft avionics applications. Some spacecraft designers fear using commercial-off-the-shelf (COTS) electronics components and systems because of susceptibility to radiation-induced failure and low reliability. The result is often an expensive custom solution using specialized components making access to space more costly.

This paper discusses an innovative technology called the "Smart Backplane" that enables the use of existing low-cost COTS electronics boards in space and mitigates the risks while maintaining the required levels of mission assurance. The "Smart Backplane" approach provides an active electronic safety net to protect against radiation induced damage at the electronics module/board level. It makes the use of high performance COTS device technology viable while dramatically lowering the costs of achieving space mission objectives (by up to 75%). The "Smart Backplane" technology provides spacecraft avionics system designers with a cost-effective way to use today's highest performance COTS electronics in mission critical applications, something that were once considered impossible. We will present the results of the radiation tests used to validate the "Smart Backplane" approach at COTS equipment level and we will discuss where this innovative technology has been selected for future mission critical launcher and human spaceflight applications.

KEYWORDS

COTS Electronics, Spacecraft Data Handling, Spacecraft Avionics, Single Event Effect, Single Event Latch-Up, Radiation Tolerance, Re-Entry Vehicle, Upper Stage, Smart Backplane.

INTRODUCTION

When it comes to space vehicle engineering, whether it is a launcher, a re-entry vehicle or a satellite, the tolerance of on-board electronics to radiation effects can be one of the most challenging aspects of the system design. The risk of on-board electronic equipment failure due to the radiation effects depends on orbit trajectory and duration that determines the exposure to trapped radiation as well as solar and cosmic radiation sources. The overall impact at equipment level is determined by a complex interaction of shielding, circuit design, device technology & particle energy spectra and the tolerance to radiation effects is one of the key criteria for selecting the on board equipment and sub-systems.

In recent times, with increasing demands to get more out of limited budgets, designers of spacecraft systems have been motivated to find ways to mitigate against radiation effects within the scope of limited program budgets but without compromising the overall Mission Assurance requirements. This paper will discuss how a novel approach to radiation mitigation at board level, as opposed to component level, allows the use of existing high performance Commercial Off the Shelf (COTS) electronics systems in a space radiation environment, thereby lowering the cost involved in the design, certification, manufacture and deployment of such a system.

SPACE RADIATION ENVIRONMENT EFFECTS

The space radiation environment consists of highly energetic Protons, Electrons and Heavy Ions. Figure 1 shows the two main sources of space radiation – the Sun and galactic cosmic rays. Semiconductor components are essential building blocks of modern spacecraft electronics. As radiation interacts with a semiconductor it produces ionization which effectively increases the conductance of the material. As a result, ionizing radiation creates tiny spikes of electrical current in the material. Cumulatively, these current spikes cause degradation of material characteristics and are known as Total Dose Effects. Individually, they can temporary or permanently disturb the function of a device, a phenomena known as Single Event Effects (SEE).

A good analogy to help understand radiation effects in spacecraft electronics is to think about it in terms of the tyre on a car where total dose is the equivalent of general wear-and-tear from road use, whereas Single Event Effect is the equivalent of a puncture.

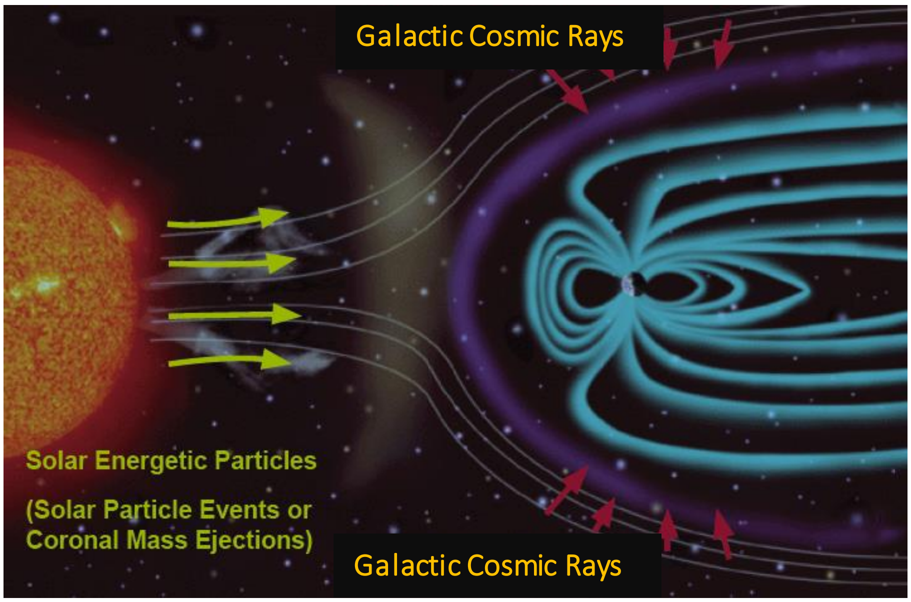

Exhibit 1: Sources of Space Radiation (Image Credit: NASA)

Total Dose Effects

The amount of radiation dose, i.e. the amount of radiation deposited in the material in a given period of time, that results in ionization is called Total Ionizing Dose (TID). The total dose accumulated during a space mission depends on the orbit and duration of the mission. Ionization of a semiconductor material typically causes very small leakage currents, which can lead to negative long-term consequences. The total dose effects cause a slow degradation of a component's performance, such as threshold voltage shift or decrease in switching speed, and eventually lead to component failure.

Single Event Effects

The increased density of integrated circuits has resulted in the size of the elementary semiconductor structures shrinking to the level where a spurious current spike produced by a single particle can disrupt the operation of the circuit. These disruptions are commonly known as Single Event Effects (SEE), and while there are a number of classifications of event types we will deal with the following two types of SEE.

• **Single Event Upset (SEU)** - occurs when a radiation-induced current causes a memory structure to change its state. This results in a temporary error in device output or its operation and is commonly referred to as "soft error". In the case of an SEU, the device is not damaged and will function properly in the future, but the data processed by the device can be corrupted.

• **Single Event Latch-Up (SEL)** - occurs when a radiation-induced current activates a parasitic structure (e.g. transistor), which forms an undesired low-impedance path in the semiconductor structure. It disrupts proper functioning of the circuit, and if not corrected, can possibly even lead to its destruction due to overcurrent. The circuit typically remains latched up until is powered off and afterwards it may continue function properly.

Radiation Testing of Spacecraft Electronic Equipment

When designing electronic equipment for a spacecraft it is essential for the designer to have a good understanding of the environment the spacecraft will operate in, as this will influence the scope of their design. This includes an understanding of anticipated total dose as well as the density and energy of particles that may cause SEE during the mission. The equipment is then typically tested to verify it performance in a space radiation environment through a series of standardized tests. These tests include TID using Gamma Radiation, Proton Irradiation using a Synchrotron source and Heavy Ion irradiation using a source of heavy ions. The test thresholds (Pass / Fail criteria) for single event effects on equipment performance are typically driven by the spacecraft mission requirements.

SINGLE EVENT LATCH-UP (SEL) DETECTION & MITIGATION

In mitigating radiation effects, the aim is to reduce risk – i.e. an attempt to either eliminate or reduce the probability of a radiation-induced event occurring or to limit the consequences to the system if the event occurs.

There are several common methods employed in electronics design to reduce the effects of radiation on vehicle data handling equipment. Broadly speaking, there are three approaches to address radiation in space electronics design:

a) Improved material hardness
b) Infrastructure design techniques to improve radiation tolerance
c) Software methods to improve radiation tolerance

These include techniques employed at both an electronics level as well as a system-level. The most effective form of mitigation will depend on the scope of the mission under consideration and the expected type and duration of radiation exposure. The different types of mitigation are summarized in Exhibit 2 & outlined in the following sections.

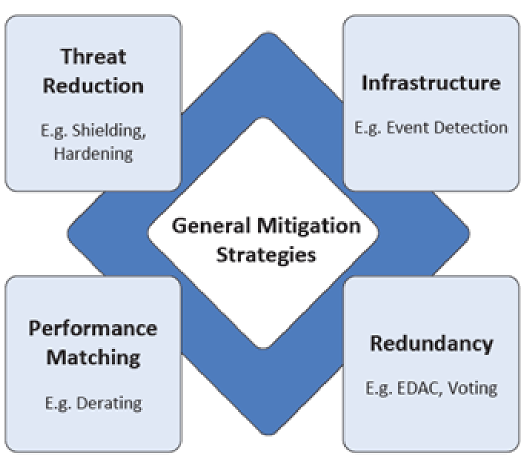

Exhibit 2: General categorization of system-level radiation mitigation techniques

Mitigation of Total Dose Effects

Total Dose Effects in spacecraft electronics can be minimized with physical shielding, component de-rating and through conservative circuit design.

Shielding

One option to protect electronics from radiation effects is to introduce a protective physical 'shield' around an electronic circuit design. Shielding is the practice of reducing the radiation dose experienced by an electronic circuit by blocking the radiation with physical barriers (e.g. Aluminum or Tungsten) that absorb radiation before it gets to the sensitive electronic components. Shielding is a very effective technique for reducing the impact of electron and low-energy proton dose. However, it generally does not reduce the threat of SEEs caused by high-energy cosmic rays. In fact, thick shielding can have the opposite effect entirely and increase the SEE rate because of the creation of multiple secondary particles due to interactions between the cosmic rays and the shield material. Shielding also incurs a weight penalty – given the current associated cost of access to space (It cost in the region of $15-20,000 for every kilo of equipment sent to the International Space Station), this may make shielding prohibitive in terms of providing a radiation protection for all electronics.

De-Rating & Conservative Circuit Design

Fundamentally, de-rating is the operation of an electronic circuit at less than its rated maximum power in order to improve reliability and prolong its operational life. In some cases, a device that is functional but has some parameters exceeding specifications after TID testing can be de-rated if the out-of-spec parameters do not affect circuit function and are not radically increasing as the dose is increased.

Single Event Latch-Up Detection and Mitigation

Latch-up protection is typically implemented as an watchdog circuit designed to protect the electronic circuit from a latch-up event. The objective of latch-up mitigation is to allow proper system operation after a latch event. If a latch-up is likely to occur frequently in a mission-critical circuit, then mitigation should include full protection against device damage, automatic recovery from latch-up, and resumption of normal system operation. Depending on the design of the protection circuitry, this may not be sufficient on its own as a mitigation technique.

Logic Redundancy as Mitigation

Sequential logic such as finite state machines and counters also contain memory elements that may be susceptible to SEUs. These memory elements continuously drive logic, and an upset can easily propagate widely through a circuit. In a common approach to SEU mitigation, logic memory elements such as flip-flops are reproduced three times (triplicated), and a voting circuit is used to continuously detect and correct any SEU. Recent families of radiation-tolerant Microsemi FPGAs, widely used in space electronics, implement this mitigation within the core logic function such that the designer does not need to explicitly include redundant logic in their design. Redundancy and voting techniques also can be used to mitigate SEUs in microprocessors. For example, multiple microprocessors can be run in lockstep, with all outputs compared and voted to ensure that only proper values are used. However, resynchronization of a processor affected by an SEU is a complex procedure.

Use of Radiation Hardened Components

Previously, we have described several different design techniques that individually mitigate against the effects of TID and SEE – there is another option available for electronic system designers that is based on device technology and not on circuit design. This involves the use of radiation hardened or "space grade" electronic components throughout their designs. Radiation hardening is the technology of making electronic components and systems resistant to damage or malfunctions caused by ionizing radiation in space environments, or even in earth-based applications around nuclear reactors and particle accelerators.

Radiation-hardened components are based on their non-hardened equivalents, with some design and manufacturing variations, normally at the logical function block level, that reduce the susceptibility to radiation damage. For instance, this can be achieved with purpose-developed ASIC cell libraries, whereby the cells have already been hardened with layout techniques and/or choice of substrate.

Due to the extensive development and testing required to produce a radiation-tolerant design of a microelectronic chip, radiation-hardened chips tend to lag behind their non-hardened counterparts by anything up to 5 years and cost an order of magnitude more. There's also an issue with rad-hard electronics design in that certain components may not be available in rad-hard variants (e.g. high density memories), making it impossible to meet with the functional requirements of the system.

High performance electronics functionality can be very difficult to replicate with rad-hard components – if a non rad-hard component can be used in parallel with an appropriate mitigation technique, this can provide a marked improvement in system performance that may even be mission enabling.

Therefore, even though a rad-hard approach to space electronics systems design will address the radiation tolerance requirements of a given mission, there is a substantial investment required both in design and manufacture that may not address the budgetary and time constraints of a mission or indeed the functional requirements of the system in question.

THE CURTISS-WRIGHT SPACE COTS APPROACH

As discussed in the previous section, the lowest-risk method to prevent radiation damage is by using hardened components throughout the system design. This will ensure that the system will continue to function as expected with a high degree of immunity to the space radiation environment. However, there are drawbacks to this approach, the most significant being the cost and time associated with device hardening and with no guarantee that the design will meet with the functional requirements.

At the other extreme, you have the 'Buy-and-Fly' approach where a spacecraft avionics designer opts to build a system from COTS commercial components that meet with the functional requirements and other environmental requirements of the mission (vibration, shock, temperature etc.). The designer uses the radiation tolerance inherent in the design – most commercial components are radiation tolerant to several krad – with the expectation that the system will continue to function in a space radiation environment for a period of time, trading this low cost approach with reliability.

However, is there a middle ground between these two extremes where the reliability and mission assurance requirements of a system are not compromised while at the same time respecting the constraints of program budget and schedule requirements. This is the Space COTS approach that has been adopted by Curtiss-Wright and which is described in the following section.

Aerospace Flight Test Heritage

For the last 25 years, Curtiss-Wright has been supplying the Acra KAM-500 – a modular rugged data acquisition and recording system – to the flight test market. The basic building block of these systems is a fixed volume rugged chassis which can accept up to 13 COTS modular FPGA based data acquisition cards to gather data from a variety of sensor types

Inherent in the design of the KAM-500 are features that actively mitigate against SEU effects. The main feature is what is known as the acquisition cycle. The KAM-500 operates as a collection of synchronized FPGA based state machines that follow a schedule which occurs once per acquisition cycle. As part of the acquisition cycle, the RAM is refreshed. Therefore any SEUs that occur in RAM are overwritten within one acquisition cycle time. An acquisition cycle time could be anywhere from 100 microseconds up to 2 seconds in length.

Flight Test to Spacecraft Electronics – The Smart Backplane Innovation

However, standard components are still susceptible to SELs. In order to mitigate against SELs, Curtiss-Wright has designed the 'Smart Backplane' chassis. The Smart Backplane chassis is a rugged 12-user Slots chassis that has been designed for data acquisition in a radiation-intensive environment. Its design allows the use of COTS interface plug-in modules while at the same time preventing against the harmful effects of ionizing radiation.

Radiation Mitigation and the Smart Backplane – a Combination of Techniques

The chassis backplane is based on a robust design that is not susceptible to SEUs or SELs – this is the only place in the design where "space-qualified" components are used. All plug-in COTS modules are manufactured with commercial components but are protected by the Smart Backplane. It functions in such a way that it can detect an SEL event on a user-module and correct for that event before any damage can be done, thereby ensuring normal data acquisition is resumed without component damage and with minimal data loss. The system recovers from the SEE, and normal operation of the entire data handling sub-system is not compromised, thereby meeting with the mission assurance requirements of a space vehicle.

The system design doesn't seek to prevent radiation events – rather to quickly detect and correct for these events when they happen with no damage to the equipment and most importantly, the mission assurance, safety and reliability requirements are met.

This design allows the user to have standard plug-in COTS modules in a space environment without the need for those modules to have radiation-hardened components themselves, thereby minimizing the cost of the overall system and leveraging the use of over 100 plug-in modules already designed for data acquisition in aircraft flight testing. The possibilities for radiation-hardened data acquisition are endless. There are a wide range of sensor and actuator interfaces and data buses already available.

DETECTION OF AND RECOVERY FROM SINGLE EVENT LATCHUP

The KAM-500 is a COTS networked data acquisition system originally designed for flight test applications. The system is highly modular, consisting of common chassis and over 100 plug-in modules for interfacing with various sensors and avionic busses.

Each KAM-500 chassis can accommodate up to 13 interface plug-in modules and a single backplane controller module. The controller module controls the transfer of data across the KAM-500 backplane. Each module can be read from and written to through the data backplane. The transfer of data among individual modules is entirely controlled by the controller module. Additionally, each KAM-500 chassis has a built in power supply unit that provides five secondary voltages to each of 14 module slots. The KAM-500 backplane is passive and only facilitates the transfer of digital signals among the modules and distribution of secondary voltages.

KAM-500 based data handling systems have been deployed across more than 300 aeronautical and space platforms, from light UAVs, through helicopters, fighter jets and passenger aircrafts to launchers and re-entry spacecraft. Due to its robust FPGA based state-machine design and considered selection of EEE parts, the KAM-500 is highly reliable and immune to radiation effects when operated in a low-orbit space environment.

In order to further improve the performance of KAM-500 system in mission critical space applications, a new variant of KAM-500 with an in-situ radiation induced latch-up protection, has been developed. The Smart Backplane variant of KAM-500 chassis employs an active electronic safety net to protect against radiation induced effects at the module level.

The design of KAM-500 Smart Backplane provides a cost-effective mechanism for detecting Single Event Latch-Up through the monitoring power consumption of individual modules hosted in the KAM-500 chassis. If an anomaly in the power consumption profile of a hosted module is detected, the Smart Backplane initiates the failure isolation and recovery of the affected module. This approach does not require any modification of the existing modules housed within the chassis, neither does it have a negative impact on the performance of the system. The architecture of KAM-500 Smart Backplane is illustrated in Exhibit 1.

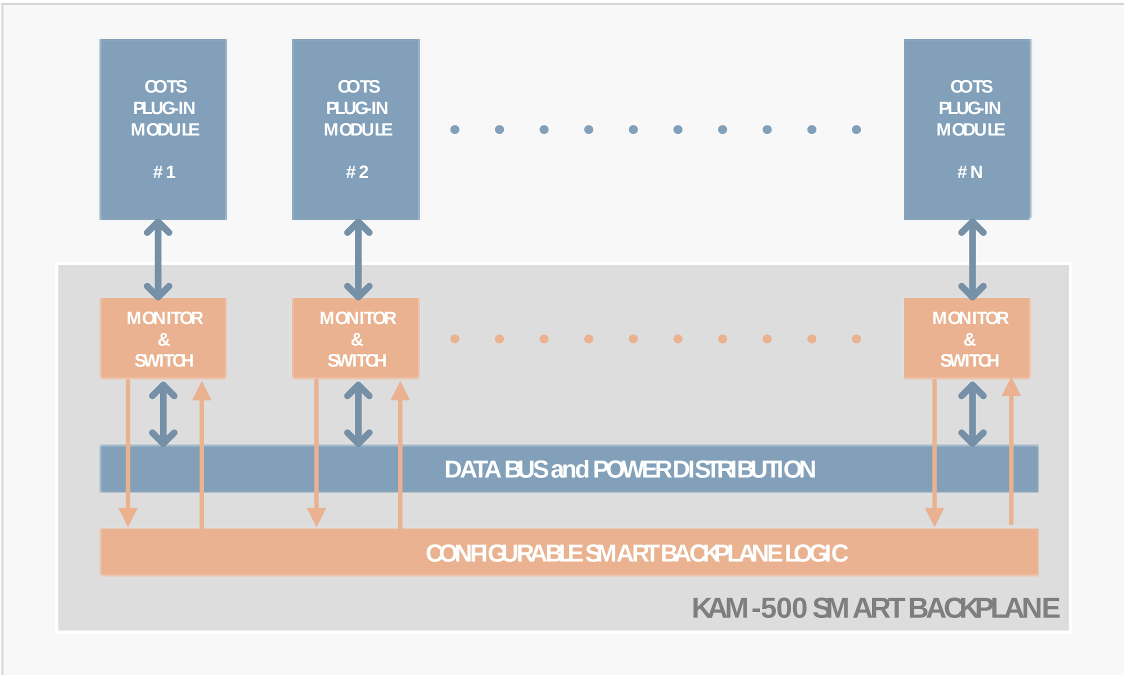

Exhibit 3: KAM-500 Smart Backplane architecture

Each module slot in the KAM-500 Smart Backplane features a monitoring and switching circuit. The monitoring circuit facilitates the measurement of power consumed by the hosted plug-in module. The switching circuit controlled by the Smart Backplane logic allows the plug-in module to be disconnected from the data bus and power lines when an anomaly in the power consumption profile is detected. The slot is re-activated after a pre-defined recovery interval.

The KAM-500 Smart Backplane is highly configurable using an user-friendly software. Power consumption limits are set by the user individually for each secondary voltage line of each module slot, together with the desired duration of the recovery interval.

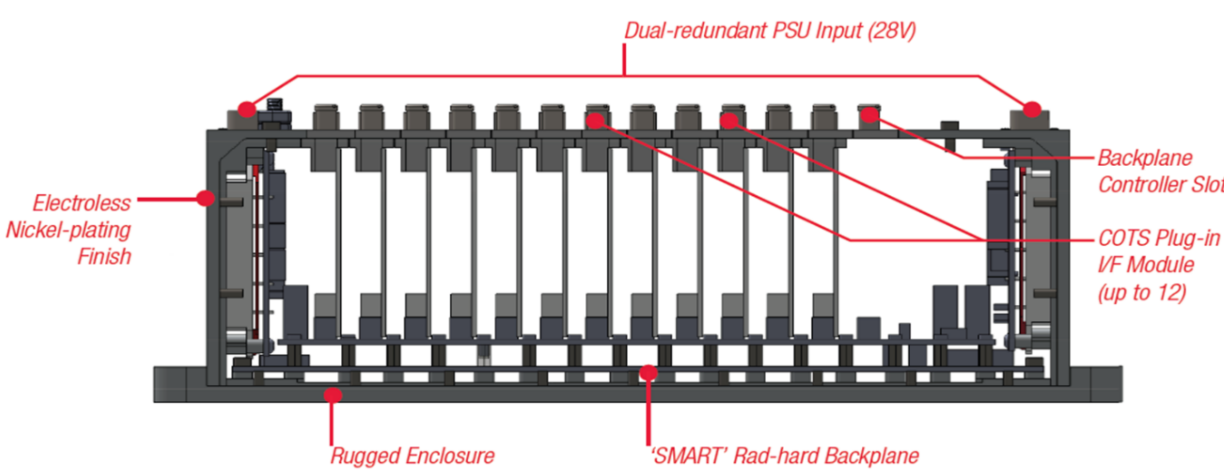

Exhibit 4: Cross-section of KAM-500 Smart Backplane chassis populated with plug-in modules

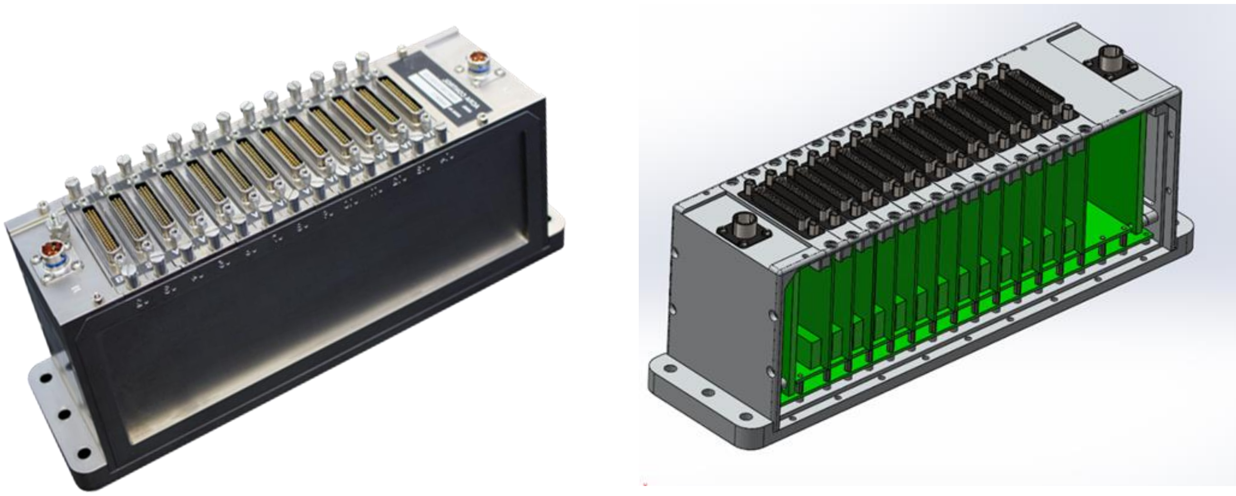

Exhibit 5: KAM-500 Smart Backplane chassis populated with plug-in modules

SMART BACKPLANE RADIATION TEST RESULTS

The design of KAM-500 Smart Backplane has been verified through a series of radiation tests. The KAM-500 Smart Backplane was successfully tested with high-energy protons and heavy-ions at the following facilities:

Test Description	Test Facility	Test Date
200Mev proton test	Proton Irradiation Facility, Paul Scherrer Institute, Switzerland	June 2014
200Mev proton test	Massachusetts General Hospital, MA, USA	May 2015
Heavy ion (Krypton) test	NASA Space Radiation Laboratory, Brookhaven National Lab, NY, USA	May 2015
200Mev proton test	Proton Irradiation Facility, Paul Scherrer Institute, Switzerland	May 2016

Exhibit 6: KAM-500 Smart Backplane Radiation Tests – Facility and Date Summary

During each test, individual KAM-500 plug-in modules were irradiated while hosted in the KAM-500 Smart Backplane chassis. The functional performance of each test article was continuously monitored and any failures and interrupts were recorded.

Exhibit 7: KAM-500 module hosted in KAM-500 Smart Backplane chassis during the radiation tests

Several Single Event Latch-Up's (SEL's) were observed on each test article during the radiation tests. Each event was successfully detected by the Smart Backplane and the impact on the system was subsequently mitigated by the Smart Backplane recovery cycle. During all tests the Smart Backplane successfully protected hosted modules from a permanent failure induced by radiation and each module performed nominally at the completion of the tests after multiple radiation induced events that resulted in power cycling by the Smart Backplane. The test results are summarized in the following table:

Test Article	Proton Test [200Mev]		250MeV Krypton Test [250MeV with LET of 4.2MeV/mg.cm^2]	
	Fluence [p/cm^2]	SEL Events	Fluence [ion/cm^2]	SEL Events
KAM-500 Controller module	1×10^{10}	56	5×10^5	30
KAM-500 Interface module	1×10^{10}	15	5×10^5	36

Exhibit 8: KAM-500 Smart Backplane Radiation Test Results – Summary Table

Note: Total data loss from a typical data acquisition module due to power cycling of the module by the Smart Backplane due to the induced SEL events for the duration of the radiation tests was approximately 2%.

BENEFITS OF THE SMART BACKPLANE APPROACH

Improved FDIR for COTS Based Systems

The Smart Backplane technology implements an innovative board level FDIR (Failure Detection Isolation and Recovery) approach for COTS electronics in spacecraft data acquisition avionics systems. It provides autonomous failure detection at board level and can isolate the board from the system without the intervention of spacecraft operators. For example if the overcurrent condition is detected on the same board repeatedly for a pre-set number of times the Smart Backplane will isolate the power supply to that board permanently to prevent propagation of the failure. The status of the board is then reported in the health & status portion of the telemetry stream.

Power Management

The Smart Backplane approach to SEL protection of COTS boards also provides the spacecraft operator to manage the power consumption and hence the energy budget of the spacecraft through the control of the power supply to individual boards or modules in the data acquisition system.

This ability to change the power on/off status of individual boards can be managed by the Smart Backplane by either of the following approaches;

- A command routed to the equipment over the Network via SNMP
- As the result of a pre-selected set of conditions (e.g. Timer, Parameters)

This approach to power management at module level provides the spacecraft designer with the ability to manage the sensor location mapping on spacecraft with a higher granularity resulting in significant cost savings in sensor harnessing mass and integration complexity at system level.

Life Cycle Cost Saving

The Smart Backplane combined with high performance COTS electronics boards has enabled spacecraft designers and operators to make significant cost savings in all aspects of the spacecraft life cycle in three main areas;

- **Use of High Performance COTS Boards in Space Radiation Environment** - The Smart Backplane permits the use of high performance COTS electronics boards in a space radiation environment while maintaining the spacecraft mission assurance requirements and provides a significant saving with respect to meeting these requirements using radiation tolerant or hard technologies at the component level.

- **Reducing Number of Avionics Boxes through Integration of Functions** - Accommodate spacecraft avionics sub-systems functions as low cost COTS modules / boards within the Smart Backplane chassis e.g. Power Switching, Signal Routing, Recording, Sat Navigation Receiver etc. saving the cost of accommodating these functions in separate avionics boxes.

- **Grouping Sensors & Reducing Harness Mass/Cost** - Groups of sensors from specific locations on spacecraft routed to modules in co-located Smart Backplane data acquisition units permits the management of power only to modules required through each mission phase saving on sensor harnessing & integration cost.

Cost Saving Case Study

The impact of implementing a Smart Backplane approach to accommodating COTS electronic boards in a spacecraft data acquisition and telemetry system that operates in a Low Earth Orbit environment (e.g. Re-entry Vehicle, Launcher Upper Stage, ISS etc.) is potential loss of up to 2% of telemetry data (based on radiation test results) as modules are power cycled by the Smart Backplane due to SEL events but with a cost saving of up to 75% over alternative approaches (based on feedback from end-users).

NEXT STEP

The next step in improving the Smart Backplane is the planning, execution & analysis of a comprehensive suite of radiation tests for Curtiss-Wright KAM-500 COTS electronics modules. This will provide the data to provide a full understanding of the behavior of our COTS equipment in a wide range of radiation test conditions (e.g. energy levels, particle types, shielding, dose level etc.) stimulating a full range of Single Event Effects will provide the information necessary for completing reliable and credible space mission design using Curtiss-Wright COTS equipment in the future, ultimately lowering the cost of delivering space missions.

CONCLUSION

The global space sector is looking to benefit from the lower cost of applying of COTS electronics equipment in ever more demanding space radiation environments and increasing levels of mission criticality. Designers of electronics for space applications can take several approaches to designing systems that can survive the effects of radiation. While using fully radiation hardened designs may yield the most protection, it is also the most expensive option. The innovative Smart Backplane chassis, developed by Curtiss-Wright, allows the use of high-performance COTS data acquisition user-modules in radiation-intensive space applications, lowering the cost of such a system by up to 75% while still meeting with the mission reliability requirements and minimizing the loss of telemetry data due to radiation events to less than 2% for a typical LEO application. The radiation tolerant Smart Backplane KAM-500 data acquisition system has already been selected for deployment in mission critical spacecraft avionics systems for manned and un-manned re-entry vehicles as well as launcher upper stages and is being considered for the instrumentation system on future planetary re-entry vehicles and as the basis for low cost COTS based small satellite avionics systems.

